REMARKS

Claims 1-29 are pending in the application. Claims 1-15 have been withdrawn from consideration. Claims 16-29 are rejected. Accordingly, claims 16-29 remain pending in the present application. Applicant includes a Petition for Extension of Time to extend the deadline for filing a response by two (2) months from December 20, 2002 to February 20, 2003.

Title of Application

Examiner states,

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The title of the patent application has been amended to "A Buried Power Buss for High Current, High Power Semiconductor Device" to clearly indicate the invention to which the claims are directed.

Cross-Related Applications Information

Examiner states,

The cross-related applications information should be updated. Appropriate correction is required.

The cross-related application text in the application has been updated in accordance with the Examiner's instructions.

Abstract

Examiner states,

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The abstract has been amended in accordance with Examiner's instructions.

Drawings

Examiner states,

The drawings are objected to because figures 17 to 20 should be labeled "Prior Art." Correction is required.

This application contains Figures 1-12. There are no figures 17-20 in this patent application. Furthermore, there are also no prior art figures in the application.

Rejections According to U.S.C. §112

Examiner states,

Claims 17 to 20 and 26 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 17, the use of "or" recite alternative structures. It is unclear and confusing to what structure is meant to be claimed.

In claim 26, it is unclear and confusing to what is meant by "a first meal covers one-half of the slot."

Any of claims 17 to 20 and 26 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

In respect to Examiner's rejection, claim 17 has been amended to delete the reference to [or Boron Up Diffusion] to make clear what structure is meant to be claimed. Claim 26 has also been amended to change "meal" to "metal" to correct a typographical error. With these amendments to claims 17 and 26, the rejection under 35 USC §112 of claims 17-20 and claim 26

has been overcome.

Rejections According to 35 U.S.C. §102

Examiner states,

Claims 16 to 20 and 23 to 27, insofar as some of them can be understood, are rejected under 35 U.S.C. §102(b) as being anticipated by Muyajima et al. (U.S. Patent #6,020,600).

For example, in claim 16, Miyajima et al. (figures 1 to 17) specifically figure 1 show a semiconductor device comprising a semiconductor substrate 1,2, the semiconductor substrate including a plurality of device structures thereon; and an interconnect on the semiconductor substrate, the interconnect comprising at least one slot 9 provided in the semiconductor substrate and at least one metal 13a, 13b within the slot.

For example, in claim 23, Miyajima et al. (figures 1 to 17) specifically figure 1 show a high current, high power interconnect on a semiconductor comprising: at least one slot 9 provided in the semiconductor substrate 1,2; and at least one metal 13a, 13b within the slot.

Applicant respectfully disagrees. Miyajima et al. disclosed a silicon carbide semiconductor device having blocking voltage, low loss and low threshold voltage and low leakage current. The Examiner has stated that an interconnect comprising "at least one slot 9 provided in the semiconductor substrate and at least one metal 13a, 13b within the slot." The trench 9 of Miyajima includes gate electrode layers 13a which are covered by an insulating layer. Hence Applicant submits that firstly this element of Miyajima is not an interconnect slot. Secondly, a metal within a slot, as recited in the present invention in claims 16 and 23 is different from a gate electrode layer on a trench with an insulating layer thereupon as disclosed in Miyajima. For these reasons claims 16 and 23 are allowable over the cited references.

Claims 16, 17, 23 and 24 insofar as some of them can be understood, are rejected under 35 U.S.C. §102(b) as being anticipated by Kawakami et al. (U.S. Patent #5,929,482).

For example, in claim 16, Kawakami et al. (figures 1 to 16) specifically figure 1 show a semiconductor device comprising: a semiconductor substrate 1, the semiconductor substrate including a plurality of device structures thereon; and an interconnect on the semiconductor substrate, the interconnect comprising at least one slot 6 provided in the semiconductor substrate and at least one metal 11 within the slot.

For example, in claim 23, Kawakami et al. (figures 1 to 16) specifically figure 1 show a high current, high power interconnect on a semiconductor substrate 1 comprising: at least one slot 6 provided in the semiconductor substrate; and at least one metal within the slot.

Initially, and with respect to claims 21, 22, 28 and 29, note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case makes clear.

Applicant respectfully disagrees. Kawakami discloses a power semiconductor device and a method for manufacturing the same. Similar to Muyajima, Kawakami does not disclose an interconnect. The trench 6 includes a conductive layer 11 which is utilized as part of the device structure. The trench is the device structure. Accordingly, the present invention, as recited in claims 16 and 23, is not taught or suggested by cited references.

Rejections under 35 USC §103

Applicant submits that claims 18-22 and 24-29 are allowable since they depend from allowable base claims.

References listed but not applied

The listed references are cited as of interest to this application, but not applied at this time.

Applicant has reviewed the references cited as of interest and find them to be no more relevant than the applied references.

Conclusion

Therefore, for the above identified reasons, the present invention as recited in independent claims 16 and 23 is neither taught nor suggested by the cited reference. Applicant further submits that claims 17-22 and 24-29 are also allowable because they depend on the above

allowable base claims.

In view of the foregoing, Applicant submits that claims 16-29 are patentable over the cited reference. Applicant, therefore, respectfully requests reconsideration and allowance of the claims as now presented.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

Applicants' attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE

Please change the title of the application as follows:

Buried Power Buss for a High Current, High Power Semiconductor Device[s and a Method for Providing the Same]

IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 2, with the following rewritten paragraph:

The present application is related to the following listed two applications: Serial No. 10/034,067, filed on 12/28/2001 [_____ (2208P)], entitled "Buried Power Buss Utilized As A Sinker for High Current, High Power Semiconductor Devices and A Method for Providing the Same;" and Serial No. 10/034,279, filed on 12/28/2001 [_____ (2209P)], entitled "Buried Power Buss Utilized As A Ground Strap for High Current, High Power Semiconductor Devices and A Method for Providing the Same"; assigned to the assignee of the present application[, and filed on the same date].

IN THE CLAIMS

16. (Amended) A semiconductor device comprising:

a semiconductor substrate, the semiconductor substrate including a plurality of device structures thereon; and

an interconnect on the semiconductor substrate, wherein the interconnect is not part of the device structure, the interconnect comprising at least one slot provided in the semiconductor substrate and at least one metal within the slot.

23. (Amended) A high current, high power interconnect on a semiconductor substrate comprising:

at least one slot provided in the semiconductor substrate; and

at least one metal within the slot, wherein the interconnect is not part of any of a plurality of device structures on the substrate.

24. (Amended) The high current, high power interconnect of claim 23 wherein the semiconductor substrate comprises:

a substrate region; and

an epitaxial (EPI) layer over the substrate region, wherein the plurality of device structures are provided in the EPI layer.

26. (Amended) The high current interconnect of claim 25 wherein the plurality of metals comprises two metals, a first metal covers one-half of the slot and a second metal fills the slot.

IN THE ABSTRACT

Please replace the Abstract, beginning on page 29, line 2, with the following Abstract:

A method and system for providing an interconnect on a semiconductor device is disclosed. The method and system comprises providing a semiconductor substrate with a plurality of device structures thereon and providing at least one slot in the semiconductor substrate. The method and system include providing a metal within the at least one slot.

This first metal in a preferred embodiment consists of three depositions of metal when sputtered, with the first two depositions being buried in the silicon prior to a dielectric and a third deposition of what is called the first metal layer. This third deposition provides the normal interconnect pattern as it normally is patterned in standard metalization schemes.

[In a preferred embodiment, the interconnect consists of a combination of a buried power buss and interconnect layer that, when employed properly, provides the following advantages:

1. Slotted metal having an oxide jacket surrounding it, thus allowing the metal to be connected randomly while isolating itself from other circuit functions.

2. Low interconnect sheet resistance available per function performed.

3. Low Ron X Area for a given area, where Ron is the on resistance of a Bipolar Transistor, or an MOS transistor (when used in a CMOS or BiCMOS configuration).

4. Provides an oxide isolated ground strap that is an ideal short to ground.

5. Provides ground strap throughout the integrated circuit wherever isolation is required between components.

6. Provides a metalized sinker for connecting the collector of a BiPolar transistor to the buried layer, or a metalized drain for connecting the drain to the buried layer of a CMOS device; thus ensuring the lowest collector or drain resistance.

7. Provides a metalized sinker and ground strap while eliminating the masking and long time, high temperature isolation diffusion that is in standard processing.

8. Provides a metalized sinker and ground strap while eliminating the masking and long time, high temperature sinker diffusion.

9. When the epitaxial layer is less than 6 microns thick it allows the buried layer masking to be eliminated.

10. Oxide isolation in place of junction isolation results in lower leakage and lower

capacitance thus providing a method for improved performance of high frequency, low power devices.

11. Low interconnect sheet resistance that allows for reduced interconnect RC time constants and therefore faster operation.

12. Low interconnect sheet resistance for high current, high power operation of integrated circuits.

13. Significant improvement in heat transfer over standard or damascene methods of metalization and interconnect.

14. Reduced current density in critical parts of the operation of the integrated circuit over standard approaches and other approaches used at this time.

15. Improved electromigration by an order of magnitude due to the improvement in heat transfer and reduced current density.

16. Elimination of isolation and sinker processes in integrated circuits.

17. Significant reduction in the die size for a given function since the isolation and sinker are provided by the buried power buss which is oxide isolated; thus allowing the isolation and sinker to move much closer to other active areas of Bipolar, MOS, DMOS, CMOS and passive components.

18. Significant reduction in de-biasing of emitter, collector, drain in high current applications due to the increase of cross section of metal through the use of this buried power buss. This results not only in a higher gain in these active circuit components, but also wider current range.

19. More gross die per wafer due to the reduction of die size and other savings. Since defect density is a function of area this approach results in less defects due to the reduction in the area of the die and higher yield. This combination of more die per wafer and lower yield loss

results in more net die per wafer for a given function when using the buried power buss.

20. Due to improvement in de-biasing, the improvement in heat transfer, and the smaller die; the resulting die is viable in a smaller package and therefore opens up new markets.

21. All these functions and improvements are provided by a single masking process that provides the slots that are oxidized and metalized, while dropping process steps that are numerous, long in process time, and at high temperatures. This results in an integrated circuit process that is very low in Root Dt (square root of the diffusion constant times time). It is a proven fact that processes carried on at lower temperatures reduces the chance for defect introduction and propagation.

22. Due to the improved heat transfer, die using this approach are able to work at higher power dissipation before being limited by secondary breakdown.

23. Due to the thicker metal in the bonding pads there is increased protection against ESD failures as well as providing an improved bonding reliability.

24. The buried power buss is able to supply thick low sheet resistance metal to both the emitter and collector on Bipolar power devices to prevent de-biasing and provide low Ron resistance of the power output transistor.]